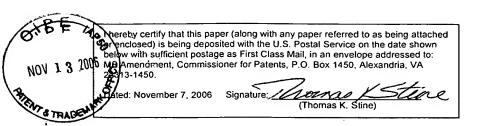
The 2/83



Docket No.: 29898/41747

(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Shimura Hiroshi

Application No.: 10/562,767

Filed: April 3, 2006 Art Unit: 2183

For: Method for Forming a Parallel Processing

System

Examiner: Not Yet Assigned

Confirmation No.: 3983

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT (IDS)

MS Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 CFR 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached PTO/SB/08. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Supplemental Information Disclosure Statement is filed before the mailing date of a first Office Action on the merits as far as is known to the undersigned (37 CFR 1.97(b)(3)).

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter

Application No.: 10/562,767 Docket No.: 29898/41747

filed in this application by this firm) to our Deposit Account No. 13-2855, under Order No. 29898/41747. A duplicate copy of this paper is enclosed.

Dated: November 7, 2006

Respectfully submitted,

Thomas K. Stine

Registration No.: 32,310

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PTO/SB/08A/B (09-06)
Approved for use through 03/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known		
				Application Number	10/562,767-Conf. #3983	
			SCLOSURE	Filing Date	April 3, 2006	
			APPLICANT	First Named Inventor	Shimura Hiroshi	
				Art Unit	2183	
			necessary)	Examiner Name	Not Yet Assigned	
heet	1	of	1	Attorney Docket Number	29898/41747	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.1	Document Number Number-Kind Code ² (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	

		FOREI	GN PATENT	DOCUMENTS		
Examiner Initials*	Cite No.1	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		CA 2 448 549	11-28-2002	IPFlex Inc.		1
		EP 1 416 388	05-06-2004	IPFlex Inc.		1

^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. \(^1\) Applicant's unique citation designation number (optional). \(^2\) See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. \(^3\) Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). \(^4\) For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. \(^5\) Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. \(^6\) Applicant is to place a check mark here if English language Translation is attached.

		NON PATENT LITERATURE DOCUMENTS	
Examiner Initials	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		BABB et al., "The Raw Benchmark Suite: Comutation Structures for General Purpose Computing," IEEE J. Comp. Soc., Sec. 3.1, PP. 134-143 (1997).	
		CHEN et al., "A Reconfigurable Multiprocessor IC for Rapid Prototyping of Algorithmic-Specific High-Speed DSP Data Paths," <i>IEEE J. Solid-State Circuits</i> , 27:1895-1904 (1992).	
		CHEN et al., "An Integrated System for Rapid Prototyping of High Performance Algoritm Specific Data Paths," <i>IEEE Comput. Soc.</i> , pp. 134-148 (1992).	
		COMPTON et al "Reconfigurable Computing: A Survey of Systems and Software," ACM Computing Surveys, 34:171-210 (2002).	
		CRONQUIST et al., "Architecture Design of Reconfigurable Pipelined Datapaths," IEEE Comput. Soc., Sec. 1 and 2.1, pp. 23-40 (1999).	
		CRONQUIST et al., "Specifying and Compiling applications for RaPiD," IEEE Comput. Soc., Secs. 3 and 4, pp. 116-125 (1998).	
		HAUSER et al., "Garp: A MIPS Processor with a Reconfigurable Coprocessor," IEEE Comput. Soc., pp. 24-33 (1997).	
		MIRSKY et al., "A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources," IEEE Comput. Soc., Sec. 2.2:157-166 (1996).	
		SINGH et al., "MorphoSys: An Integrated Reconfigurable System for Data-Parallel and Computation-Intensive Applications," <i>IEEE Transactions on Computers</i> , 49:465-474 (2000).	
		Supplementary European Search Report for European patent application No. 04746469.8 - 2224 dated August 10, 2006.	

^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Examiner	Date	
Signature	Considered	

¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.